Organic Junction Field-Effect Transistor

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The realization and performance of a novel organic field-effect transistor—the organic junction field-effect transistor (JFET)—is discussed. The transistors are based on the modulation of the thickness of a depletion layer in an organic pin junction with varying gate potential. Based on numerical modeling, suitable layer thicknesses and doping concentrations are identified. Experimentally, organic JFETs are realized and it is shown that the devices clearly exhibit amplification. Changes in the electrical characteristics due to a variation of the intrinsic and the p-doped layer thickness are rationalized by the numerical model, giving further proof to the proposed operational mechanism.

1. Introduction

Since the invention of the organic field-effect transistor (OFET) in the early 1980s,[1] the performance of these devices has increased steadily.[2] Nowadays, OFETs are used in prototypes of e.g. active matrix backplanes[3] or flexible RFID tags.[4] However, progress was mainly driven by an increase in mobility of the semiconducting material, and less progress has been made in the development and optimization of alternative transistor structures.

For inorganic semiconductors many variants of the standard metal-oxide-semiconductor field-effect transistor (MOSFET) such as the function field-effect transistor (JFET) and the metal semiconductor field-effect transistor (MESFET) are known.[5] Both, JFETs and MESFETs are based on the control of a depletion zone in a doped layer, which modulates the conductivity of the channel. In MESFETs, the depletion zone is formed by a Schottky-junction, whereas in JFETs the modulation of the thickness of a depletion zone in a pn junction is used to control the transistor channel. Due to their large transconductance, silicon based JFETs are used for example in high input-impedance operational amplifiers, in constant current sources, and to switch analogue signals. For organic electronics, JFETs would have additional advantages. In particular, no (inorganic) gate insulator is required, reducing fabrication complexity. Furthermore, organic JFETs could be less prone to gate bias stress, which is believed to be caused by interface states at the interface between the organic layer and the inorganic gate insulator.

However, although organic MESFETs have been reported in the scientific literature,[6,7] organic JFETs (OJFETs) are thus far unknown, which is mainly due to the significant technological challenges of such a transistor. In particular, a well controllable doping technology has to be developed in order to define pn junctions with adjustable depletion zones. For organic semiconductors, such a doping technology has mainly been used in the field of organic optoelectronics,[8–10] and is by far less established in the field of organic transistors. However, recently we were able to show that the depletion zone in organic pin junctions can be tuned by the doping concentration in the doped layer, the thickness of the intrinsic layer, and the reverse voltage applied to the device,[11,12] which is the most fundamental requirement for the realization of an organic JFET.

In this publication, we describe the design of an organic junction FET based on our organic doping technology. The design of the transistor is guided by numerical modeling of the pin junction. It is also discussed, how the major challenge, the control of reverse currents flowing in the pin diodes, can be solved. We present data showing that the devices operate as a variable resistor and reach amplification.

2. JFET Principle: Design Guided by Simulation

The setup of the organic JFET is shown in **Figure 1**. The devices consist of Al gate electrodes, 50 nm of BPhen n-doped with Cs, an intrinsic interlayer of NPB (15–30 nm), a thin layer of pentacene doped with the p-dopant F_6-TCNNQ at a concentration of 4 wt% (15–30 nm), and finally source and drain contacts consisting of 30 nm Au and 50 nm Al. The transistors have a channel length of 150 μm and a channel width of 20 mm, the overlap of source and gate or drain and gate is approx. 0.84 mm^2.

The operation of the JFET can be understood as follows: the p-doped pentacene layer forms a conductive channel between the source and the drain. The resistance of this channel (without gate voltage applied) is given by the thickness of the layer and its doping concentration. To modulate the resistance, a voltage is applied between the source and gate electrode, i.e., across the nip diode consisting of n-BPhen, NPB, and p-pentacene. The voltage is applied in reverse direction of the pin junction, which depletes the p-doped pentacene and the n-doped BPhen layer.

In **Figure 2** this behavior is illustrated by a qualitative simulation of the pin junction consisting of 50 nm n-BPhen, 25 nm NPB, and 20 nm p-pentacene operated in reverse direction. Instead of providing quantitative results, the simulation aims

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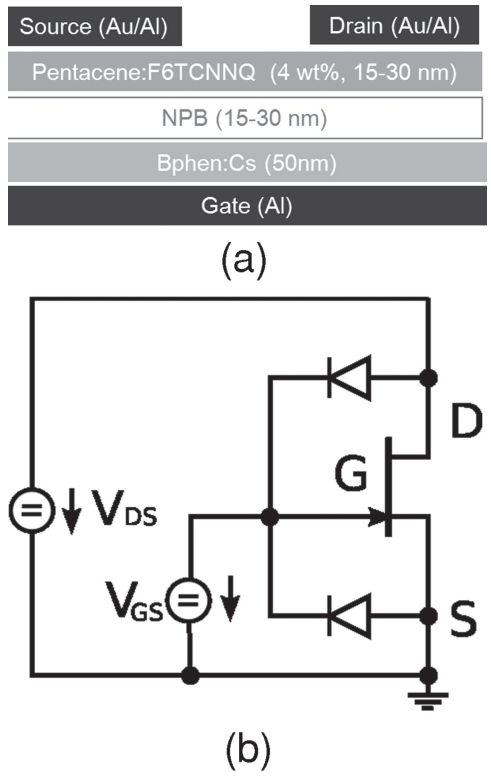

Figure 1. Setup of the organic junction field-effect transistor. (a) Layer structure and (b) circuit diagram including diodes due to overlap between source or drain and gate.

to predict trends in the device operation to be compared to the experiments discussed in the remainder of this manuscript. The simulation is based on a self-consistent solution of Poisson's equation and the Fermi integrals in the organic layers. The parameters used for the simulation of the pin junction are summarized in **Table 1**. The resulting level diagram of the junction for 0.8 V and –0.2 V is shown in Figure 2a. As expected, a thin depletion zone is formed at the interface cathode/n-doped BPhen, which generates a quasi-ohmic contact and efficient injection of electrons. On the other hand, the injection of holes at the anode on the right is ohmic as the HOMO of pentacene and the work-function of gold align, so that the p-pentacene is not depleted at this interface.

If the reverse voltage is increased, the levels of the p-pentacene layer shift toward higher energies, leading to an increased electric field in the intrinsic layer and the formation of a depletion zone in the p-pentacene layer, visible by an increased level bending at the interface NPB/p-pentacene. This effect is also visible in the plot of the charge carrier density vs. the position in the device for different reverse voltages (Figure 2b). For larger voltages, the p-doped layer is increasingly depleted. In contrast to the hole density, the density of electrons is not strongly affected by the applied voltage, which is due to the significant larger doping density in the n-layer, leading to a vanishing small depletion layer width at the interface n-BPhen/NPB.

The results are summarized in Figure 2c, where the depletion layer width (defined as the position where the density of holes drops to 1/e of the doping density) is plotted vs. the

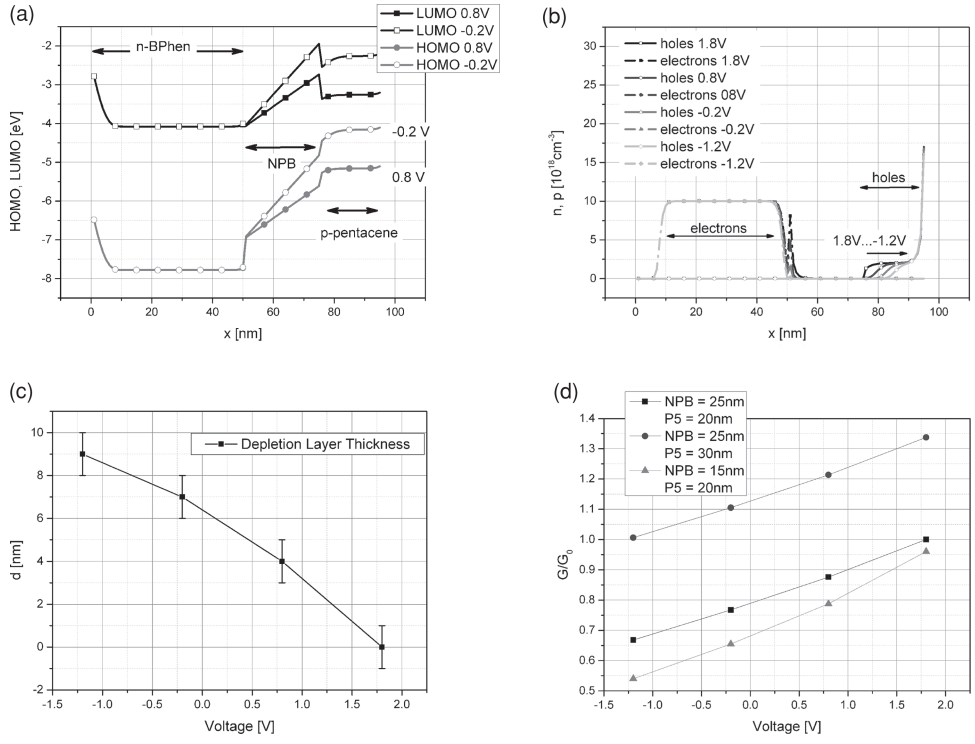

Figure 2. Modeling the organic pin junction of the JFET. In (a) the level diagram of the junction at 0.8 V and at –0.2 V is shown. (b) displays the charge carrier density in the junction at different voltages. It can be seen that the p-layer is increasingly depleted (c). The increase in depletion layer thickness leads to a modulation of the conductance G of the p-pentacene layer, shown in (d).

Table 1. Simulation Parameter (ε_r =3 for all layers).

Material	HOMO [eV]	LUMO [eV]	Work function [eV]	Density of active n-dopants [cm^{-3}]	Density of active p-dopants [cm^{-3}]
Al			−4.2		
BPhen:Cs	−6.1[17]	−2.4[17]		10^{19}	0
NPB	−5.4[a)]	−2.52		0	0
Pentacene:					
F_6-TCNNQ	−5.1[a)]	−3.2		0	$2 \cdot 10^{18}$
Au			−5.1		

[a)] Determined by UPS.

applied voltage. As expected, the depletion layer thickness increases with applied voltage. The maximum depletion layer thickness is 10 nm.

The increased depletion layer thickness leads to a modulation of the channel conductance shown in Figure 2d. The conductance is calculated under the assumption of vanishing small drain-source voltages, i.e., for a constant potential along the channel. The conductance is normalized to the conductance measured at 0 V applied between gate and source voltage and is determined assuming a proportionality of the conductance to the number of free charge carriers, i.e., neglecting any field or charge carrier dependence[13,14] of the mobility. As shown in Figure 2d the conductance drops by approx. 35% at a voltage of −1.2 V.

A strength of the JFET is the precisely tunable device characteristic. Two examples, the decrease in intrinsic layer thickness from 25 to 15 nm and an increase in p-pentacene layer thickness from 20 to 30 nm, are shown for comparison in Figure 2d. The decrease in intrinsic NPB layer thickness leads to a slight increase in gate modulation, which can be explained by the smaller voltage drop across the intrinsic layer and in consequence the larger voltage drop across an increased depletion layer. However, the increased depletion layer thickness leads to a decrease in overall current. On the other hand, an increase in the thickness of the p-pentacene layer leads to an increase in conductance.

These simulations suggest that it is possible to realize an organic JFET, where the resistance of the p-doped pentacene layer can be modulated by the applied gate voltage. However, in contrast to organic field-effect transistors and to the assumption of the simulation, gate currents cannot completely be avoided, as the reversely biased pin diode will always show leakage currents. Furthermore, if the voltage exceeds the breakthrough voltage, the current in backward direction sharply rises due to a Zener-like tunneling effect[11] limiting the maximum gate voltage, which can be applied between gate and drain or gate and source. Furthermore, as our transistor design shows a significant overlap between source/drain and gate electrode, parasitic, reversely biased pin junctions have to be considered in the discussion of the results, which is also highlighted in the equivalent circuit of our setup shown in Figure 1b. Thus, to experimentally realize a working OJFET, it is essential to precisely control the backwards currents.

3. Organic pin Diodes: Control of Reverse Currents

The characteristic of the source/gate or drain/gate diode is shown in **Figure 3**. The diodes consist of 60 nm Al, 50 nm BPhen doped with Cs at a doping concentration yielding a conductivity of $1.6 \cdot 10^{-5}$ S/cm, an intrinsic layer of NPB (15, 20, 25, 30 nm), a thin layer of pentacene doped with the p-dopant F_6-TCNNQ (or F_6-TNAP[10]) at a concentration of 4 wt%, and a second electrode consisting of 30 nm Au and 50 nm Al. The thickness of the p-doped pentacene layer varies slightly from 15 nm to 25 nm, which, however, has no influence on the diode characteristic (see Supporting Information, Figure S1).

The current in reverse direction, i.e., at negative voltages, strongly decreases with increasing intrinsic layer thickness. This result is in accordance to previous reports showing that the reverse currents are due to a tunneling of electrons from occupied states in the HOMO to unoccupied states in the LUMO of neighboring molecules.[11] If the intrinsic layer thickness is increased, the electric field in the intrinsic layer as well as the tunneling probability decreases, leading to decreased backward currents. Thus, thicker intrinsic layers are preferred in order to reduce gate leakage in our devices. However, as seen in Figure 2d an increased interlayer thickness leads to a decrease in gate control of the JFET. Therefore, a compromise has to be found and we choose an interlayer thickness of 25 nm.

Besides the characteristic of the pin junction in Figure 3a the current flowing between source and drain with disconnected gate terminal is shown. As expected, the current decreases with decreasing thickness of the doped pentacene layer. The currents shown in Figure 3b correspond to a conductivity of the doped pentacene layer of 10^{-3} S/cm.

4. Operation of the Organic Junction Field-Effect Transistor

Figure 3b shows the current flowing between source and drain through the p-doped pentacene layer. In the following, it will be shown that the conductance of this layer can be modulated by an applied gate voltage, as proposed by the modulation of the depletion layer thickness seen in the simulation results shown in Figure 2.

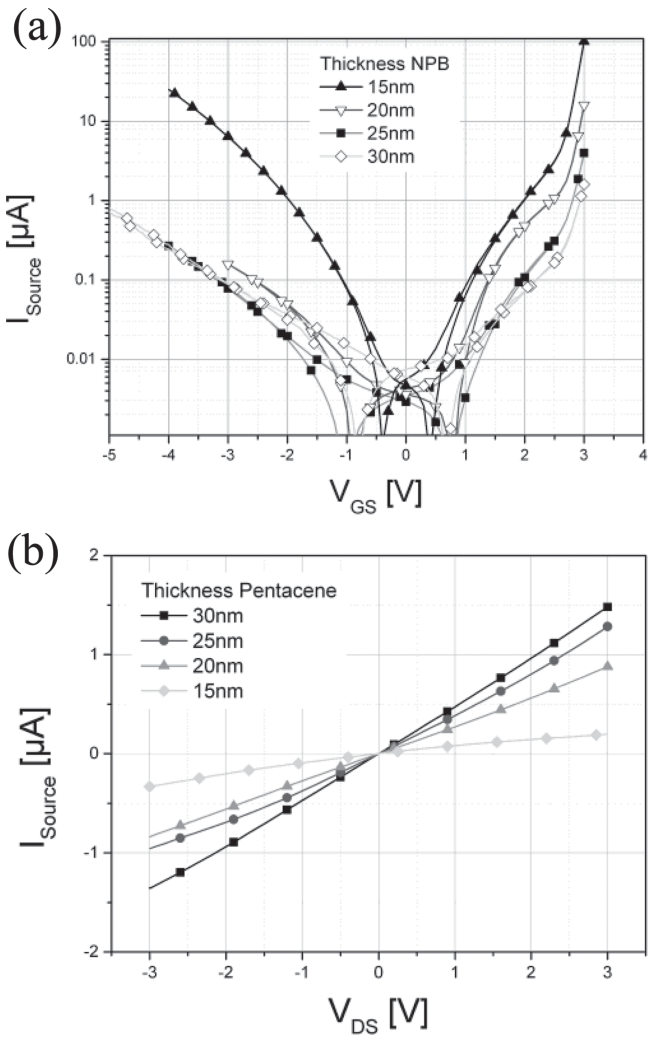

Figure 3. (a) Characteristic of the organic pin junction of the OJFET. Current flowing between source and gate of the device are plotted with the drain disconnected. Positive voltages correspond to a more positive potential of the source with respect to the gate. (b) Current flowing between source and drain with disconnected gate for different pentacene layer thickness. The characteristic corresponds to a conductivity of 10^{-3} S/cm.

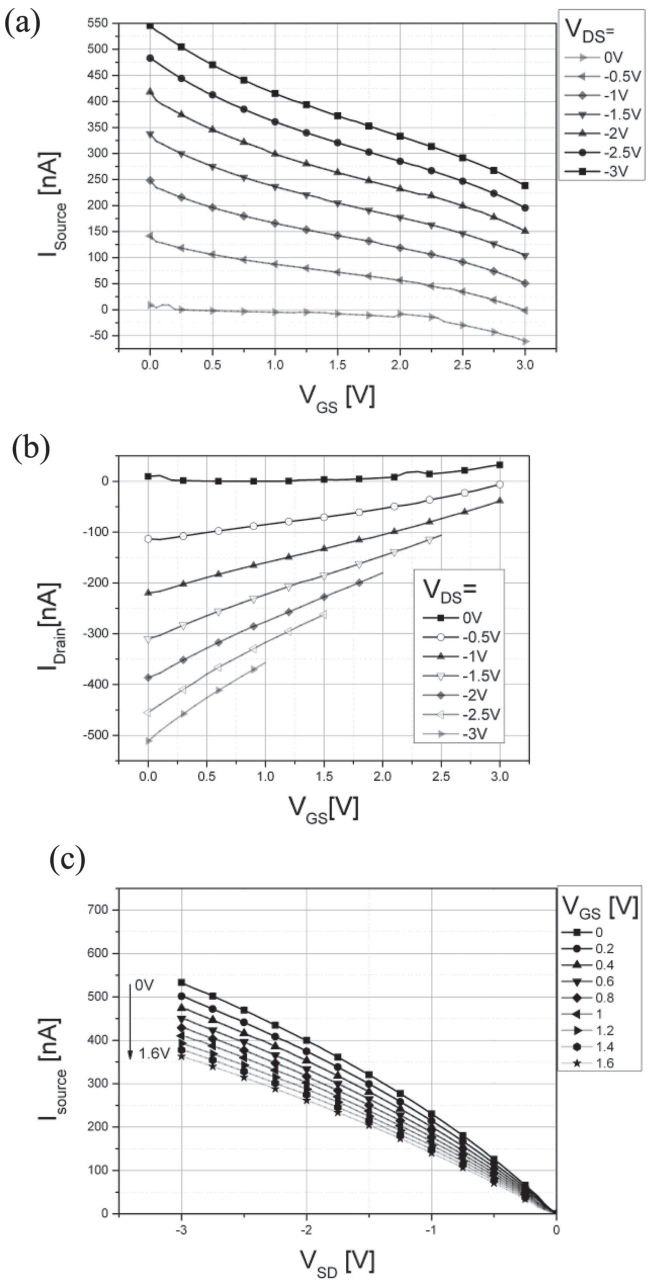

Figure 4. Characteristic of an organic JFET consisting of 50 nm n-BPhen, 25 nm NPB and 20 nm p-pentacene. In (a) the transfer characteristic is plotted (source current I_{Source} vs. gate potential), which shows gate control of the source currents. Drain currents (corrected for the parasitic currents flowing between drain and gate) are displayed in (b) and (c) shows the output characteristic.

The transfer characteristic of a transistor consisting of 25 nm intrinsic NPB layer and 20 nm of p-doped layer is shown in **Figure 4**a. As expected for a JFET, the source currents decrease with increasing gate potential, i.e., with increasing depletion of the channel. In qualitative agreement to the simulation, the currents decrease by a factor of 2 (V_{DS} = −3 V) to 5 (V_{DS} = −1 V) upon application of a gate-source voltage of 3 V (gate modulation). The drain currents qualitatively follow the same trend as the source currents, but due to the higher potential of the drain compared to the source, currents flowing in reverse direction through the parasitic diode between the spatial overlap of drain and gate (cf. the equivalent circuit in Figure 1b) are superimposed to the currents flowing into the channel. These currents are in parallel to the current flowing from source to drain. Therefore, to discuss the behavior of the JFET consistently, we subtracted the current flowing through the parasitic diode (i.e. the currents given in Figure 3a) from the drain current, yielding a corrected drain current of the JFET. The result is shown Figure 4b and the uncorrected currents are given in the (Figure S2). As expected, the drain currents decrease with increasing gate potential, which is due to an increase in thickness of the depletion zone thickness. The transconductance of the JFET $g_m = \frac{\partial I_{Drain}}{\partial V_{GS}}\Big|_{V_{DS=const}}$ is in the range of 0.1 µS.

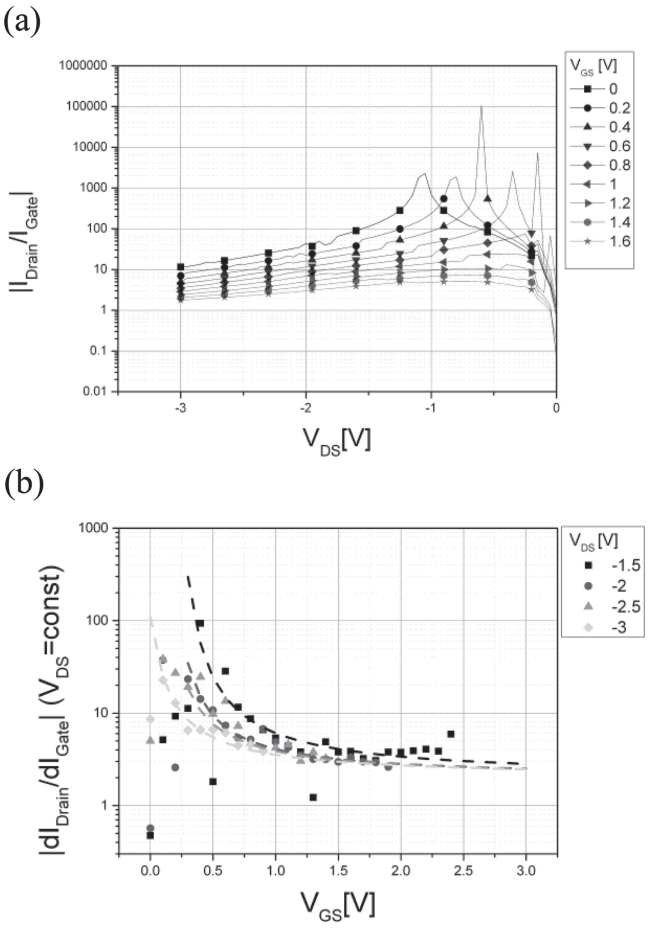

Figure 5. Amplification of the JFET: (a) absolute amplification I_D/I_C, (b) differential amplification dI_D/dI_C. The lines in (b) are to guide the eye.

The output characteristic of the transistor is displayed in Figure 4c. At small drain-source voltages the channel behaves like a normal resistor, i.e., the source current varies linearly with the voltage. However, at larger voltages the currents do not saturate, which is in accordance to the simulation result showing that a full depletion of the p-doped layer is not possible.

Unlike in ideal OFETs, gate currents are present in these devices. Therefore, it is essential to show that the device exhibit amplification, i.e., that the drain currents exceed the gate currents ($I_{Drain}/I_{Gate} > 1$) and that the differential amplification $\left.\frac{dI_{Drain}}{dI_{Gate}}\right|_{V_{DS=const}}$ exceeds unity as well. Both quantities are shown in **Figure 5**. The absolute amplification (Figure 5a) has its maximum at low V_{DS} (approx. 1 V) and decreases for higher voltages, which is mainly due to increased currents through the reversely biased diode between drain and gate. The same trends can be seen for the differential amplification shown in Figure 5b, i.e., a high amplification at small V_{DS} and a decrease in amplification for larger V_{DS}. Again, as in Figure 4b, the drain and gate currents are corrected for parasitic currents flowing due to the overlap between drain and gate. Both, absolute and differential amplification show amplification over the whole voltage range, clearly demonstrating the operation of the device.

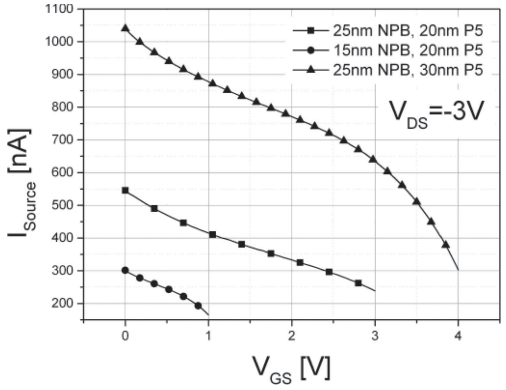

Figure 6. Variation of the JFET structure. Decreasing the intrinsic layer thickness leads to smaller currents, whereas increasing the pentacene layer thickness increases the currents as well.

5. Variation of JFET Structure

The strength of the JFET structure is its precisely tunable characteristic. The simulation shown in Figure 2d shows that I_{Source} should decrease for decreasing intrinsic layer thickness (at slightly increased gate modulation) and increase for increasing pentacene layer thickness. These trends can be confirmed by the experiment shown in **Figure 6**, where the transfer characteristic at $V_{DS} = -3$ V is shown for a JFET consisting of 25 nm NPB and 20 nm p-pentacene (the same JFET as discussed above), a JFET having a thinner intrinsic layer thickness (15 nm NPB, 20 nm p-pentacene) and a JFET with increased pentacene layer thickness (25 nm NPB, 30 nm p-pentacene). As expected from the simulation, the currents decrease for thinner NPB layer, which can be explained by a larger depletion layer thickness for the same gate potential. Furthermore, the gate currents increase and in order to keep the gate currents to an acceptable level, V_{DS} has to be limited to 1 V. Increasing the pentacene layer thickness leads to increased currents, which is due to the larger conductance of the layer. However, the gate modulation is slightly decreased to a factor of approx. 1.6 (ratio of current at $V_{GS} = 0$ V and $V_{GS} = 3$, $V_{DS} = -3$ V).

6. Conclusion

The design and realization of a novel organic transistor—the organic junction field-effect transistor—has been discussed. Using electrical modeling we are able to predict general trends of the device and to choose the correct range of layer thicknesses and doping concentrations. Furthermore, we can control the currents flowing through the reversely biased source/gate and drain/gate pin diode by increasing the intrinsic layer thickness. Choosing a sufficiently thick interlayer, first transistors are realized showing a gate modulation of the conductance between source/drain and amplification.

However, the transistors still need further improvement for realistic applications. A first step to reduce the gate currents is to decrease the overlap between gate and source or drain electrode. This, however, necessitates the use of advanced structuring, e.g., a lithography adapted to organic

layers,[15] but will help to unlock the full potential of this technology, e.g., low voltage operation and precisely tunable device characteristics.

7. Experimental Section

Modeling of Depletion Layer Thickness and Electric Potential in Organic pin Junctions: The simulations shown in Figure 2 are done by consistently solving Poisson's equation using a finite difference algorithm and calculating the charge carrier distributions in the layers assuming Fermi-Dirac statistic using a home-built solver. A discrete transport (HOMO or LUMO) level is assumed. Doping is introduced by a constant density of negatively or positively charged dopant molecules. The doping concentration in pentacene is set to only a few percent of the actual dopant concentration following recent results showing that the doping efficiency is in the range of a few percent.[10] The doping concentration in BPhen is calculated from the conductivity assuming a mobility of 10^{-5} cm^2/Vs as stated by Khan et al.[16] for thin layers of BPhen at low fields. However, the simulations are insensitive to the n-doping concentration as the depletion layer mainly extents into the p-layer. The junction is assumed to be ideally blocking in reverse direction, i.e., no electrons can reach the p-layer and no holes the n-layer.

Device Fabrication: All JFETs are prepared by thermal evaporation in a single chamber UHV tool of Kurt J. Lesker company at a base pressure of 10^{-7} mbar. The deposition system is equipped with a wedging tool, which allows depositing several samples with systematic variations on the same substrate in a single deposition run, which ensures best comparability of the samples. In particular, all samples discussed here are processed in the same run.

The samples consist of 60 nm of Al as gate, 50 nm of BPhen (4,7-diphenyl-1,10-phenanthroline, ABCR GmbH & Co. KG) n-doped with Cs, an intrinsic interlayer of NPB (*N,N′*-di(naphthalen-1-yl)-*N,N′*-diphenyl-benzidin, Sensient Technologies, 15-30 nm), a thin layer of pentacene (Sensient Technologies) doped with the p-dopant F_6-TCNNQ (2,2'-(perfluoronaphthalene-2,6-diylidene)dimalononitrile, Novaled AG) at a concentration of 4 wt% (15–30 nm), and finally source and drain contact consisting of 30 nm Au and 50 nm Al. The transistors are structured by shadow masks with a channel length of 150 µm and a channel width of 20 mm. Glass is used as substrate. Before transferring the samples to air, the samples are encapsulated under nitrogen atmosphere. The spatial overlap between source or drain electrodes and gate electrode is 0.84 mm^2.

Characterization: Characterization of the electrical properties of the transistors is done using a Semiconductor Parameter Analyzer Keithley 4200-SCS. Positive source (drain) currents are defined as currents flowing into the source (drain). All voltages are referenced to the source electrode, i.e., a positive V_{GS} corresponds to a potential of the gate, which is more positive compared to the source and a positive V_{DS} means that the potential of the drain is more positive than the potential at the source. All electrical measurements are performed at room temperature.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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